Organic Field Effect Transistors Based on Graphene and Hexagonal Boron Nitride Heterostructures

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Enhancing the device performance of single crystal organic field effect transistors (OFETs) requires both optimized engineering of efficient injection of the carriers through the contact and improvement of the dielectric interface for reduction of traps and scattering centers. Since the accumulation and flow of charge carriers in operating organic FETs takes place in the first few layers of the semiconductor next to the dielectric, the mobility can be easily degraded by surface roughness, charge traps, and foreign molecules at the interface. Here, a novel structure for high-performance rubrene OFETs is demonstrated that uses graphene and hexagonal boron nitride (hBN) as the contacting electrodes and gate dielectric layer, respectively. These heterostacked OFETs are fabricated by lithography-free dry-transfer method that allows the transfer of graphene and hBN on top of an organic single crystal, forming atomically sharp interfaces and efficient charge carrier-injection electrodes without damage or contamination. The resulting heterostructured OFETs exhibit both high mobility and low operating gate voltage, opening up new strategy to make high-performance OFETs and great potential for flexible electronics.

1. Introduction

The performance of OFETs is often constrained by the carrier channel mobility limited by the dielectric-semiconductor interface.[1–5] In particular, trap states, which can be induced by residual charge density in the dielectric or active layer, influence the threshold voltage, mobility, and hysteresis in the transfer characteristics. Therefore, a lot of effort have been devoted to finding a thin dielectric and organic single crystals active layer that can maintain high interface quality in combination with high gate efficiency to improve the performance of OFETs[1,2,6–9] In particular p- or n-types single crystal semiconducting active layers including rubrene, pentacene, tatracene, triisopropylsilylethynylpentacene (TIPS-pentacene), poly(3-hexylthiopene) (P3HT), *N,N*0-bis(n-alkyl)-(1,7 and 1,6)-dicyanoperylene-3,4:9,10-bis(dicarboximide)s (PDIF-CN2), tetracyanoquinodimethane (TCNQ), fullerene and others,[10–19] have excellent device properties when combined with dielectrics such as air-gap, polydimethylsiloxane (PDMS), CYTOP, and polymeric materials.[15,20–24] Newly developed dielectrics can preserve the high channel mobility of single crystal active layers by eliminating the interface defects. However, these devices present fabrication challenges such as integration, inter-diffusion of organic molecules into the PDMS, and residual organic solvent in the polymeric dielectrics that demand more practical methods for electronic applications. Recently, it was reported that hexagonal boron nitride (hBN), an insulating isomorph of graphene, is a highly optimal substrate and dielectric for graphene FETs due to its atomically flat surface and the absence of trapped interfacial charge.[25,26] For this reason, hBN can be similarly utilized as a dielectric for high performance and low-power consumption OFETs. Furthermore, hBN can be transferred by a nondestructive lithography method that has an additional

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advantage for organic single crystal OFETs because it avoids damage from organic solvents.[27–30]

In this study, we demonstrate a novel structure of high performance OFETs by stacking rubrene single crystal, graphene, and hBN, which were employed as channel, electrode, and dielectric, respectively. The stacked OFETs were fabricated by lithography-free PDMS transfer method, which allowed us to form a atomically-flat channel interface between rubrene and hBN, and efficient charge-injection graphene electrodes without contamination.

2. Result and Discussion

Rubrene single crystals were grown in a quartz tube by physical vapor transport (PVT) and subsequently transferred onto the silicon substrate with 300 nm-thick SiO_2 capping layer, using a static gun.[27,31] **Figure 1**a shows a representative rubrene single crystal. Rod-like rubrene single crystals with thickness of 100–200 nm and width of 10–50 μm were selected for fabrication of OFET devices. The longitudinal direction of rubrene crystal corresponds to the *b*-direction, which is confirmed by selected area electron diffraction (SAED) (see below for details). We used rod-like rubrene crystals for OFET devices so that all the devices used in this work have the *b*-axis of rubrene as the channel direction because it is known to have the highest mobility charge transport in rubrene due to strong π–π overlap.[27] The hBN flakes were prepared with mechanical exfoliation method on a PDMS stamp which has a step-free and clean surface (Figure 1b). We further performed atomic force microscopy (AFM) to investigate the surface morphology of rubrene and hBN. Based on the normalized histograms of surface roughness analyzed from the AFM images, the surfaces of rubrene and hBN (root mean square roughness <0.18 nm) are more than three times smoother than SiO_2 substrates (Figure 1c). It should be noted that the relatively thick rubrene crystals (>200 nm) have a number of molecular step-edges on the surface meanwhile the thin ones (<200 nm) do not have[32,33] (see Supporting Information, Figure S1). Thus, we judiciously selected rubrene crystals thinner than 200 nm for our devices. The van der Waals interaction between two ultra-flat hBN and rubrene crystals can lead to homogenously sharp interface after hetero-stacking process.[25,34]

The atomic scale quality of interface and crystal orientation of rubrene/hBN stack was also investigated using bright-field transmission electron microscopy (BF-TEM) and SAED pattern, respectively. We prepared a stack of rubrene and hBN on an amorphous carbon coated TEM grid using PDMS transfer technique. The BF-TEM image of the stack in Figure 1d indicates that there are no trapped bubbles or molecular clusters. The electron diffraction of the stacked region (Figure 1e) exhibits the overlapped rectangular electron diffraction of rubrene (*hk0*) and hexagonal electron diffraction of hBN (*0001*), confirming that rubrene and hBN are single crystals and longitudinal direction of rubrene is *b*-axis.[31]

Figure 2a shows a schematic of the device fabrication process. Single-layer graphene films (CVD-SLG) were grown by chemical vapor deposition (CVD) on copper foil as reported elsewhere.[35] CVD-SLG electrodes were transferred onto the top of the rubrene single crystal on the wafer substrate

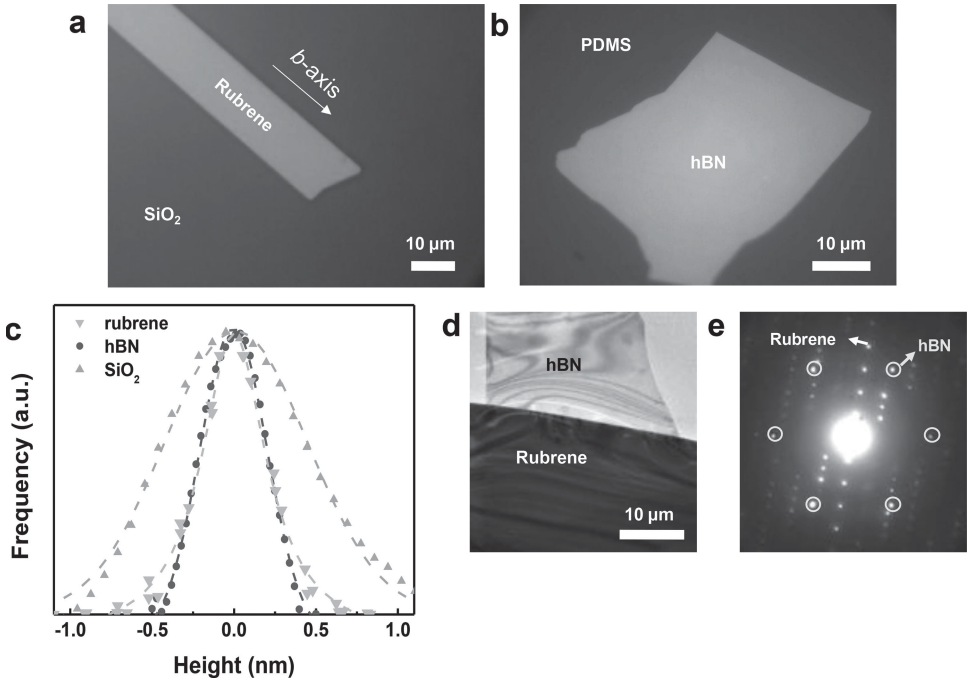

Figure 1. Optical micrographs of a) rubrene single crystal on SiO_2/Si substrate and b) hBN flake on PDMS stamp. The arrow in (a) indicates *b*-axis of the rubrene crystal. c) Histograms of height distribution measured by AFM for rubrene, hBN, and SiO_2. The AFM results indicate that the surface of rubrene and hBN is ultra-flat compared to SiO_2. d) BF-TEM image and e) SAED pattern of the stacked layers of rubrene / hBN. The circled electron diffraction spots show a hexagonal symmetry of hBN single crystal and the other spots are from rubrene single crystal.

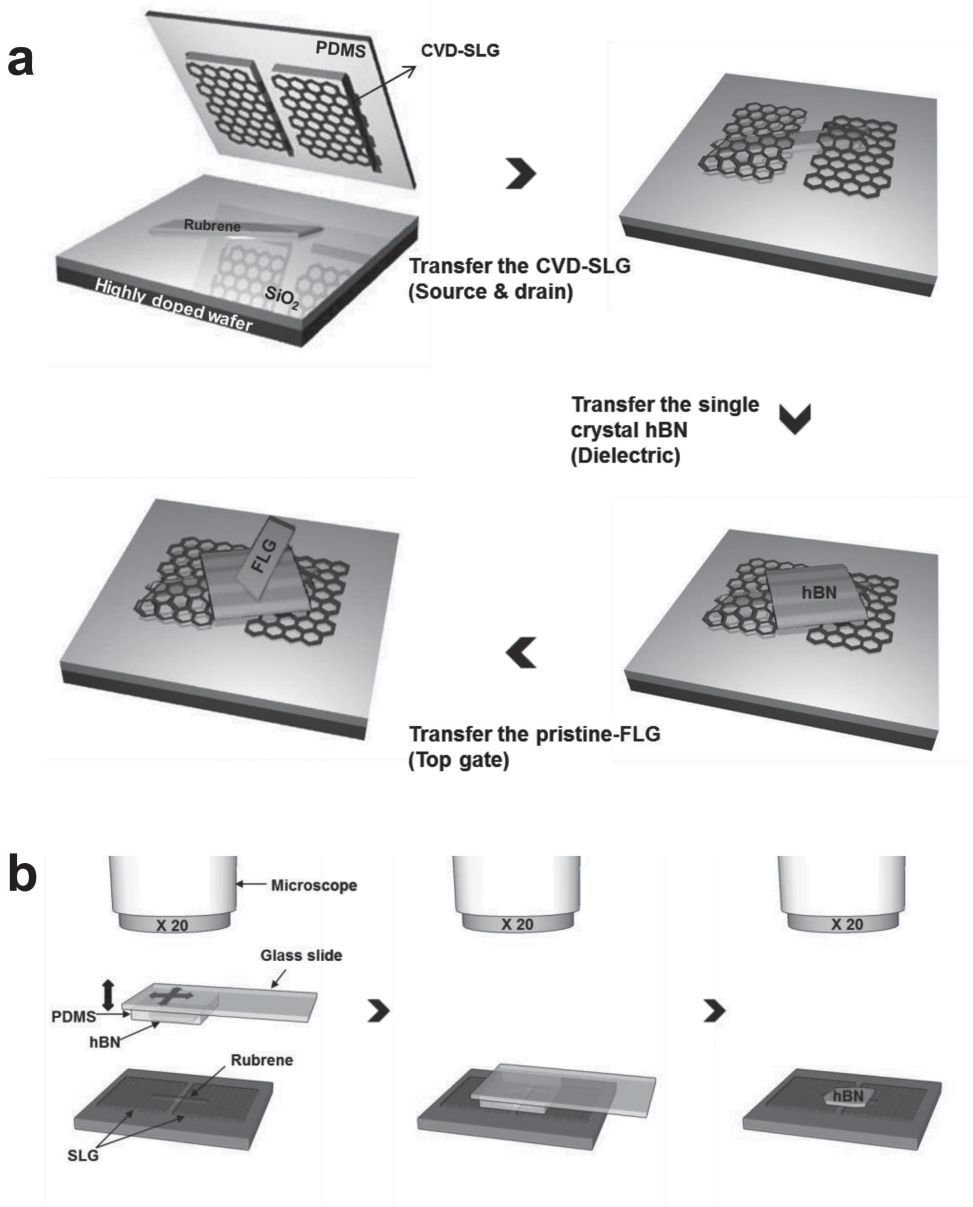

Figure 2. a) Schematic device fabrication process. Rubrene single crystal FETs were fabricated by stacking CVD-SLG, hBN, and pristine-FLG as electrodes, dielectric, and top-gate electrode, respectively. b) Schematic for alignment step in transfer process. The hBN flake is transferred onto channel region between two CVD-SLG electrodes by using three-axis micro-manipulator.

by using a patterned PDMS mold, as we have previously described.[31] Note that, during this transfer process, the channel surface of the rubrene single crystal was untouched. Then, a hBN flake on PDMS stamp was transferred onto the channel area of the rubrene single crystal using a three-axis micro-manipulator.[25,26] Following a similar method, few-layer graphene (FLG) was stacked onto the hBN flake to serve as a top-gate electrode. Figure 2b shows detailed process for aligning and transfering target flakes using three-axis micro-manipulator. The final device was heated in vacuum at 80 °C for 24 h to ensure full contact between layers. The optical micrographs in **Figure 3**a–c show the device at each fabrication step. The schematic structure of final devices is shown in Figure 3d. In this structure, a gate voltage can be applied with either the bottom-gate *p*-doped Si or the top-gate FLG. The AFM image of Figure 3e shows the morphology of the representative device of Figure 3d before transfer of top-gate FLG layer. As shown in line profile of Figure 3f, the thicknesses of the rubrene crystal and hBN flake are 170 nm and 30 nm, respectively. As already confirmed by BF-TEM (Figure 1d), the AFM image also shows no bubbles or residue in the channel interface between the rubrene and hBN layers. This stacking method obviates the need for conventional lithographic processing, which involves solvents. Therefore, we can easily fabricate devices with high reproducibilty, minimizing any damage during the process.

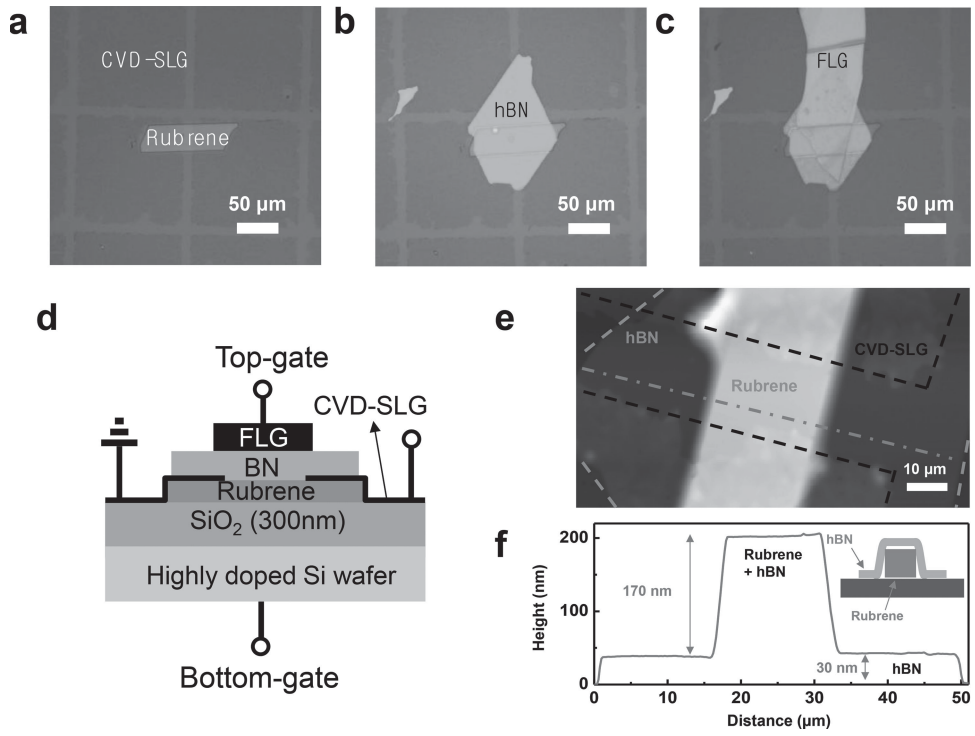

Figure 3. Optical micrographs of a) Rubrene single crystal covered by CVD-SLG electrodes, b) Channel area covered by hBN flake, and c) Transfer of top-gate pristine-FLG electrode. d) Schematic circuit diagram of the final device structure. e) AFM image of the stacked layers of rubrene/CVD-SLG / hBN on SiO_2 / Si substrate. The dashed lines indicate the border of each layer. f) Line profile measured from dash-dot line of (e). The inset of (f) shows the cross-section structure of the 30 nm thick hBN on 170 nm thick rubrene crystal.

The OFETs can be electrically tested by directly contacting the source, drain, and gate electrodes using micromanipulator probes. In particular, the device structure of Figure 3d allows us to characterize either top-gate or bottom-gate transistor geometry for direct comparison of device performance on the same rubrene single crystal. **Figure 4**a and b show transfer (I_{DS}–V_{BG}) and output (I_{DS}–V_{DS}) characteristics in the bottom gate-top contact (BG-TC) configuration measured under ambient condition. The *p*-type current modulation with operating voltage of 60 V and on/off ratio of approximately 10^4 was observed. The field effect mobility of the OFET was calculated from MOSFET standard model in the saturated regime. The estimated mobility of this BG-TC device was less than 1 $cm^2\ V^{-1}\ s^{-1}$ using the gate capacitance (11.5 nF cm^{-2}) of 300 nm thick SiO_2. Due to the vertical charge transport from the channel to the CVD-SLG electrodes in the BG-TC device configuration,[36] the mobility value is lower than that previously reported for a device with SiO_2 dielectric.[31] Moreover, for most of BG-TC devices, large shift of threshold voltage was observed, indicating that interface between rubrene single crystal and SiO_2 has a large density of trap states.[37]

In contrast, greatly improved FET characteristics were measured for the device in the top gate-top contact (TG-TC) configuration (Figure 4c and d) using similarly grown rubrene single crystals. Using the dielectric strength (7.9 MV cm^{-1})[38] and constant (ε = 3.5)[25] of hBN, the capacitance of ≈30 nm thick hBN was estimated to be ≈100 nF cm^{-2}. This value is an order of magnitude higher than that of thick SiO_2 used in the BG-TC device. This allows the TG-TC device to operate with much lower gate voltage. For this TG-TC configuration, the on/off ratio of ≈10^7 was observed at low gate voltage of 5 V. The field-effect mobilities of TG-TC OFETs extracted from the saturation regime are 10–15 $cm^2\ V^{-1}\ s^{-1}$ (from five devices, see Supporting Information, Figure S2), which are carrier density-independent. Quantitatively, we found that $I_D^{1/2} \sim V_G$ in the saturation regime, indicating uniform charge carriers and mobility along the channel.[39] The output curves in Figure 4d show *p*-type characteristics with current saturation beyond V_{DS} of −5 V with stepped gate field modulation. As shown in the inset of Figure 4d. the linear increase in drain current at small V_{DS} indicates that a junction of CVD-SLG and rubrene forms an Ohmic contact. It can be explained in terms of well-alignment between Fermi level of highly *p*-doped CVD-SLG (work function >4.9 eV, from adsorbed oxygen, moisture, and charged impurites on the SiO_2 dielectric layer) and HOMO level (≈5.4 eV) of rubrene[31,40,41] (see Supporting Information, Figure S3).[42] By contrast, the slow turn-on seen in the zoom-in output curves in the inset of Figure 4b indicates that the BG-TC device has higher contact resistance due to the vertical separation between the top contacts and the bottom conducting channel.[36] Furthermore, the TG-TC devices provides no hysteresis in the transfer curves which can be explained by the charge trap-free interface, i.e., clean hBN/rubrene interface (see Supporting Information, Figure S4). When the TG-TC device was measured in a linear regime (see Supporting Information, Figure S5a), field effect mobility increased as a function of gate voltage above threshold voltage and highest value was maintained at higher gate voltage region. This result indicates that channel/dielectric

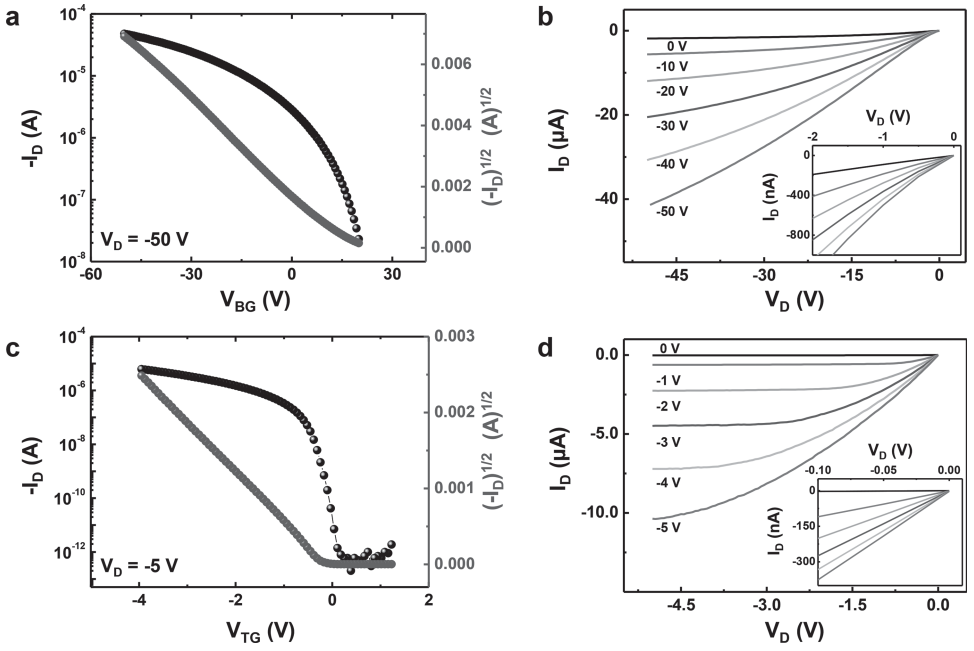

Figure 4. a) Transfer curve and b) output curves of BG-TC configuration in the fabricated rubrene FET. c) Transfer curve and d) output curves of TG-TC configuration of the same device. The insets of (b) and (d) show the zoom-in output curves at low bias region of the main panel.

interface is clean and charge carriers are uniformly generated even in a linear regime of high carrier density.[43] Whereas, the BG-TC configuration leads to the highest value near threshold voltage and decrease to very low value due to the high density of scattering charge at the interface (see Supporting Information, Figure S5b). We also found that the device performance of TG-TC configuration is more stable under ambient condition over several months, compared to other device configurations. This is probably because intimate contact of rubrene and hBN prevent any degradation of channel interface from penentration of water or gases. Furthermore, we measured the mobility as a function of temperature in TG-TC device configuration. The result exhibits that the mobility is suppressed from 15.0 cm^2 V^{-1} s^{-1} at 300 K to 6.5 cm^2 V^{-1} s^{-1} at 200 K. This result indicates that the dμ/dT value is positive (see Supporting Information, Figure S6). This positive slope may originate from the contact resistance escalation due to the contact-freezing from the two terminal measurements. Despite the positive value of dμ/dT, the mobility is still high at low-temperature which is also important for potential applications.

To verify that the observed high performance is due to the novel device configuration, OFETs with various device structures were fabricated by using different dielectrics and electrode materials. (see Supporting Information, Figure S7 and S8). Note that at least three devices for each different device configurations were fabricated and measured. Similar to previous work, rubrene single crystal FETs with air-gap dielectric and Au electrodes (Figure S7a) showed high mobility of 13–20 cm^2 V^{-1} s^{-1} as reported by other groups.[19,44,45] When different electrodes such as evaporated thin gold (20 nm, Figure S7b) or exfoliated FLG (Figure S7c) were used in bottom gate-bottom contact (BG-BC) device configuration with hBN dielectric, the mobility (3–4 cm^2 V^{-1} s^{-1}) was lower than that of the devices with CVD-SLG electrodes (see Supporting Information, Table S1). The low mobility of these devices is attributed to the residues of resist employed for e-beam lithography and bending of rubrene crystal at the edges of relatively thick electrode and hBN (device in Figure S7b). Using CVD-SLG and hBN as contacts and dielectric in a BG-BC device (Figure S7d) resulted in high mobility similar to that of TG-TC devices, but with high operating voltage. Thus, our device approach clearly shows that the TG-TC OFETs consisting of hBN, graphene and rubrene single crystals can be beneficial for low-voltage, flexible OFETs application. In addition the large area patterning of both CVD-SLG and single crystal active layers enable us to easily scale up the patterned device arrays. This will be promoted by large scale hBN that is currently investigated using CVD methods.[15,46–48]

3. Conclusion

In conclusion, we demonstrate fabrication of heterostructured OFETs consisting of rubrene single crystal, graphene, and hBN, which serve as channel, source-drain electrode and dielectric. By employing a PDMS transfer method along with hBN, atomically flat and trap-free channel interface can be produced without damaging the organic materials or contaminating the interfaces. Charge carrier injection was improved by using highly doped CVD-SLG electrodes. This straightforward and lithography-free fabrication method and novel device structure of TG-TC enable us to produce high performance OFETs with high field effect mobility, high on/off ratio, and low operating voltage by incorporating inorganic 2D materials into OFETs. This scheme opens up new strategy to make high performance OFETs by stacking 2D materials with great potential for flexible electronics.

4. Experimental Section

4.1. Growth of Materials

Rubrene single crystals were grown by physical vapor transport (PVT) as reported.[31] 2 mg of sublimed rubrene powder (>99.5%) was placed in a hot zone of the furnace. The substrate was placed in the crystallization zone (280 °C). 50 sccm of a argon (99.999%) was used as a carrier gas. After 5 minutes of pre-purging, the system was heated to 330 °C. The reaction was performed for 2 min and the system was then cooled down to the room temperature. Single-layer graphene film was grown by CVD on 25 μm-thick copper foils (Alfa Aesar, 99.8%).[35] The copper foil was heated to 1000 °C in a hydrogen flow of 2 sccm at a pressure of 50 mTorr. After annealing for 60 min, graphene was grown by introducing methane gas flow of 35 sccm while maintaining hydrogen flow. After growth at 300 mTorr and 1000 °C for 30 min, the sample was rapidly cooled to ambient temperature under a flow of methane and hydrogen. After growth, a patterned PDMS mold was attached onto the graphene, and the copper foil was etched by ammonium persulfate for 2 h.

4.2. Device Fabrication

Rod-like rubrene single crystals on SiO_2/Si substrate were selected for fabrication of OFET devices. CVD-SLG electrodes was transferred onto the top of rubrene single crystal with alignment in optical manipulator. A hBN flake was then transferred by using an unpatterned PDMS stamp. FLG was stacked onto the hBN flake by the same process to serve as a top-gate electrode. The final device was heated in vacuum at 80 °C for 24 h to ensure full contact between layers.

4.3. Characterization of Materials

AFM (XE-100, Park Systems) and TEM (JEOL, JEM-100CX) were used to characterize the interface between layers and crystallography. hBN flake was deposited onto holy carbon grid and rubrene single crystal was transferred onto it using PDMS transfer technique. TEM imaging and diffraction were conducted with low operation voltage of 80 kV to avoid any apparent damage.

4.4. Electrical Characterization of Devices

Electrical properties of fabricated devices were measured with a semiconductor parameter analyzer (Agilent, 4155C) in air and at room temperature. The graphene electrodes were directly contacted by electrical probes in a micro-manipulator probe station.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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